Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical and oral	Tutorial	Theory	Practical and oral	Tutorial	Total
ECC303	Digital Electronics	03	--	--	03	--	--	03

Course Code	Course Name	Examination Scheme							
		Theory Marks					Term Work	Practical and Oral	Total
		Internal assessment			End Sem. Exam	Exam duration Hours			
		Test 1	Test 2	Avg. of Test 1 and Test 2					
ECC303	Digital Electronics	20	20	20	80	03	--	--	100

Course Pre-requisites:
Basic Electrical & Electronics Engineering

Course Objectives:
1. To understandvarious number systems&codes and to introduce students to various logic gates, SOP, POS form and their minimization techniques.
2. To teach the working of combinational circuits, their applications and implementation of combinational logic circuits using MSI chips.
3. To teach the elements of sequential logic design, analysis and design of sequential circuits.
4. To understand various counters and shift registers and its design using MSI chips.
5. To explain and describe various logic families and Programmable Logic Devices.
6. To train students in writing programs with Verilog hardware description languages.

Course Outcomes:
After successful completion of the course students will be able to
1. Perform code conversion and able to apply Boolean algebra for the implementation andminimisation of logic functions.
2. Analyse, design and implement Combinational logic circuits.
3. Analyse, design and implement Sequential logic circuits.
4. Design and implement various counter using flip flops and MSI chips.
5. Understand TTL & CMOS logic families, PLDs, CPLD and FPGA.
6. Understand basics of Verilog Hardware Description Language and its programming withcombinational and sequential logic circuits.

Module No.	Unit No	Contents	Hrs.
1		**Fundamentals of Digital Design**	07
	1.1	**Number Systems and Codes:** Review of Number System, Binary Code, Binary Coded Decimal, Octal Code, Hexadecimal Code and their conversions, Binary Arithmetic: One's and two's complements,	
	1.2	**Codes:**Excess-3 Code, Gray Code, Weighted code, Parity Code: Hamming Code	
	1.3	**Logic Gates and Boolean Algebra:** Digital logic gates, Realization using NAND, NOR gates, Boolean Algebra, De Morgan's Theorem, SOP and POS representation, K Map up to four variables	
2		**Combinational Circuits using basic gates as well as MSI devices**	07
	2.1	**Arithmetic Circuits:** Half adder, Full adder, Ripple carry adder, Carry Look ahead adder, Half Subtractor, Full Subtractor, multiplexer, cascading of Multiplexer, demultiplexer, decoder, Comparator (Multiplexer and demultiplexer gate level upto 4:1).	
	2.2	**MSI devices:** IC7483, IC74151, IC74138, IC7485.	
3		**Elements of Sequential Logic Design**	07
	3.1	**Sequential Logic:** Latches and Flip-Flops. RS, JK, Master slave flip flops, T & D flip flops with various triggering methods, Conversion of flip flops,	
	3.2	**Counters:** Asynchronous, Synchronous Counters, Up Down Counters, Mod Counters, Ring Counter, Twisted ring counter, Shift Registers, Universal Shift Register.	
4		**Sequential Logic Design:**	07
	4.1	**Sequential Logic Design:** Mealy and Moore Machines, Clocked synchronous state machine analysis, State reduction techniques (inspection, partition and implication chart method) and state assignment, sequence detector, Clocked synchronous state machine design.	
	4.2	**Sequential logic design practices:** MSI counters (7490, 7492, 7493,74163, 74169) and applications, MSI Shift registers (74194) and their applications.	
5		**Logic Families and Programmable Logic Devices**	05
	5.1	**Logic Families:** Types of logic families (TTL and CMOS), characteristic parameters (propagation delays, power dissipation, Noise Margin, Fan-out and Fan-in), transfer characteristics of TTL NAND(Operation of TTL NAND gate),CMOS Logic:CMOS inverter, CMOS NAND and CMOS NOR, Interfacing CMOS to TTL and TTL to CMOS.	
	5.2	**Programmable Logic Devices**: Concepts of PAL and PLA. Simple logic implementation using PAL and PLA, Introduction to CPLD and FPGA architectures, Numericals based on PLA and PAL	
6		**Introduction to Verilog HDL**	06
	6.1	**Basics**: Introduction to Hardware Description Language and its core features, synthesis in digital design, logic value system, data types, constants, parameters, wires and registers. **Verilog Constructs:** Continuous & procedural assignment statements, logical, arithmetic, relational, shift operator, always, if, case, loop statements, Gate level modelling, Module instantiation statements.	
	6.2	**Modelling Examples:** Combinational logic eg.Arithmetic circuits, Multiplexer, Demultiplexer, decoder, Sequential logic eg. flip flop, counters.	
		Total	**39**

Text Books:

1. R. P. Jain, Modern Digital Electronics, Tata McGraw Hill Education, Third Edition 2003.
2. Morris Mano, Digital Design, Pearson Education, Asia 2002.
3. J. Bhaskar, A Verilog HDL Primer, Third Edition, Star Galaxy Publishing, 2018.

Reference Books:

1. Digital Logic Applications and Design – John M. Yarbrough, Thomson Publications, 2006
2. John F. Warkerly, Digital Design Principles and Practices, Pearson Education, Fourth Edition, 2008.
3. Stephen Brown and ZvonkoVranesic, Fundamentals of digital logic design with Verilog design, McGraw Hill, 3rd Edition.
4. Digital Circuits and Logic Design – Samuel C. Lee, PHI
5. William I.Fletcher, "An Engineering Approach to Digital Design", PrenticeHall of India.
6. Parag K Lala, "Digital System design using PLD", BS Publications, 2003.
7. Charles H. Roth Jr., "Fundamentals of Logic design", Thomson Learning, 2004.

Internal Assessment Test:

Assessment consists of two class tests of 20 marks each. The first-class test (Internal Assessment I) is to be conducted when approx. 40% syllabus is completed and the secondclass test (Internal Assessment II) when additional 40% syllabus is completed. Duration of each test shall be one hour.

End Semester Theory Examination:

1. Question paper will comprise of total 06 questions, each carrying 20 marks.
2. Total 04 questions need to be solved.
3. Question No: 01 will be compulsory and based on the entire syllabus wherein 4 sub-questions of 5 marks each will be asked.
4. Remaining questions will be randomly selected from all the modules.
5. Weightage of each module will be proportional to the number of respective lecture hours as mentioned in thesyllabus.